ECEN 3733 - Digital Circuit Design

Fall 2026 Syllabus, Section 01, CRN 41061,

Credit hours: 3

Instructor

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Public Instructor Information

Instructor Professional Qualifications: Ph.D. Computer Engineering, University of Pittsburgh
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Course Description

3733. Digital Circuit Design. Modern digital circuit analysis and design. Latches, flip-flops, registers, counters, memories, programmable logic arrays, and arithmetic logic units. Logic gate-level synthesis and computer simulation using CAD tools. Synchronous and asynchronous finite-state machines. Prereq.: ECEN 1521, ECEN 2633. 3 s.h.

Course Readings

Group	Title	Author	ISBN
Required	Fundamentals of Logic Design, Enhanced Edition. 7th ed.	Roth Jr , Charles; Kinney, Larry; John, Eugene.	9781337620352
Required	Asynchronous finite state machine design: A lost art?	Carroll, C.	Academic Paper

C. Carroll, “Asynchronous Finite State Machine Design: A Lost Art?,” *Asee.org*, pp. 11.258.1–11.258.8, June 2006, Accessed: Aug. 10, 2026. [Online]. Available: https://peer.asee.org/379

The course readings are subject to change in the event of extenuating circumstances, research developments, current events, and/or to ensure better learning.

Tentative Schedule

Week of	Reading(s)	Proposed Topic	Due/To Prepare for Class
8/24	Unless otherwise noted, all readings are found in the course textbook.	Unit 1. Introduction Number Systems and Conversion	Read unit
8/31		Unit 2. Boolean Algebra	Read unit
9/7		Unit 3. Boolean Algebra (Continued)	Read unit
9/14		Unit 4. Applications of Boolean Algebra Minterm and Maxterm Expansions	Read unit
9/21		Unit 5. Karnaugh Maps (Exam #1)	Read unit (Prepare for exam)
9/28		Sec. 6.6. Quine-McCluskey Method Overview; 7.1. Multi-Level Gate Circuits; 7.2. NAND and NOR Gates	Read sections listed in the "Proposed Topic" column
10/5		Unit 8. Combinational Circuit Design and Simulation Using Gates	Read unit
10/12		Unit 9. Multiplexers, Decoders, and Programmable Logic Devices	Read unit

10/19		Unit 10. Introduction to VHDL (Exam #2)	Read unit (Prepare for exam)
10/26	See the "Course Readings" section in this syllabus for a link to Carroll's paper.	Within 20.2. VHDL Test Bench and For Loop Carroll: "Asynchronous finite state machine design: A lost art?"	Read section listed Read web resource
11/2		Unit 11. Latches and Flip-Flops	Read unit
11/9		Unit 14. Derivation of State Graphs and Tables	Read unit
11/16		Unit 17. VHDL for Sequential Logic	Read unit
11/23		Unit 12. Registers and Counters	Read unit
11/30		Continue Unit 12. (Catch-up) Work on final projects (Exam #3)	Review unit (Prepare for exam)
12/7		(Finals Week)	

The course schedule, policies, procedures, and assignments in this course are subject to change in the event of extenuating circumstances, by mutual agreement, and/or to ensure better learning.