ECEN 6933 - Digital Systems: VHDL Design

Fall 2026 Syllabus, Section 01, CRN 41062,

Credit hours: 3

Instructor

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Public Instructor Information

Instructor Professional Qualifications: Ph.D. Computer Engineering, University of Pittsburgh
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Course Description

6933. Digital Systems: VHDL Design. Local minimization, design of combinational networks; design of synchronous and asynchronous sequential machines; design of digital systems using VHD, modeling combinational and sequential networks, compilation, simulation, and synthesis of VHDL codes. 3 s.h.

Course Readings

Group	Title	Author	ISBN
Required	Digital Systems Design Using VHDL	C. H. Roth Jr and L. K. John	9781305635142 (See Note 1)
Required	Asynchronous finite state machine design: A lost art?	Christopher Carroll	Academic Paper (See Note 2)
Required	7.2: Multiprocessor and Multicore Systems	Patrick McClanahan	Web resource (See Note 3)
Required	5.6: Processor Architectures	OpenStax	Web resource (See Note 4)

Note 1: To enhance your learning experience and provide discounted access to *Digital Systems Design Using VHDL*, your course is part of an inclusive access model called First Day®. You can easily access *Digital Systems Design Using VHDL* right from Blackboard.

YSU will bill you at the discounted price as a course charge for this course.

You have the option to opt-out of this program in the LMS. For more information and FAQs click here: customercare.bncollege.com (https://customercare.bncollege.com/)

Note 2: C. Carroll, "Asynchronous finite state machine design: A lost art?," in *Proc. 113th Annu. ASEE Conf. Expo.*, Chicago, IL, USA, 2006, pp. 11.258.1–11.258.11. [Online]. Available: https://peer.asee.org/asynchronous-finite-state-machine-design-a-lost-art.pdf

Note 3: Access at 7.2: Multiprocessor and Multicore Systems - Engineering LibreTexts (https://eng.libretexts.org/Courses/Delta_College/Introduction_to_Operating_Systems/07:_Small_to_Big_Systems/7.02:_1.9_Multiprocessor_and_Multicore_Systems)

Note 4: Access at 5.6: Processor Architectures - Engineering LibreTexts (https://eng.libretexts.org/Bookshelves/Computer_Science/Programming_and_Computation_Fundamentals/Introduction_to_Computer_Science_(OpenStax)/05%3A_Hardware_Realizations_of_Algorithms-_Computer_Systems_Design/5.06%3A_Processor_Architectures)

The course readings are subject to change in the event of extenuating circumstances, research developments, current events, and/or to ensure better learning.

Tentative Schedule

Day	Date	Reading(s)	Proposed Topic	Due/To Prepare for Class
Wed	8/26	Unless otherwise noted, all readings are found in the course textbook.	Ch 1: Review of Logic Fundamentals	Read chapter

Wed	9/2		Ch 1: Review of Logic Fundamentals	Review chapter
Wed	9/9		Ch 2: Introduction to VHDL	Read chapter
Wed	9/16		Ch 2: Introduction to VHDL	Review chapter
Wed	9/23		Ch 3: Introduction to Programmable Logic Devices: Intro., 3.1, 3.2, 3.3 (Exam 1)	Read chapter sections that are listed in the "Proposed Topic" column (Prepare for exam)
Wed	9/30		Ch 3: Introduction to Programmable Logic Devices: 3.4, 3.5	Read chapter sections listed
Wed	10/7		Ch 4: Design Examples: 4.2, 4.4, 4.5, 4.7	Read chapter sections listed
Wed	10/14		Ch 5: SM Charts and Microprogramming: Intro., 5.1, 5.2, 5.3, 5.4	Read chapter sections listed
Wed	10/21	See Course Readings section for link.	Ch 5: SM Charts and Microprogramming: Intro., 5.5 (and 5.6 if time allows) Carroll: "Asynchronous finite state machine design: A lost art?"" Asynchronous Finite State Machines	Read chapter sections listed Read specified web resource
Wed	10/28		Ch 9: Design of RISC Microprocessors: Intro., 9.1, 9.6 (Exam 2)	Read chapter sections listed
Wed	11/4		Ch 9: Design of RISC Microprocessors: 9.7, 9.8 (9.9 if time allows)	Read chapter sections listed
Wed	11/11		Ch 10: Verification of Digital Systems: Intro., 10.1, 10.2, 10.3, 10.4, 10.5, 10.6	Read chapter sections listed
Wed	11/18		Ch 11: Hardware Testing and Design for Testability: Intro., 11.1, 11.4, 11.7	Read chapter sections listed
Wed	11/25		(Thanksgiving Break)	
Wed	12/2	See Course Readings section for links.	McClanahan: 7.2: Multiprocessor and Multicore Systems. OpenStax: 5.6: Processor Architectures (Exam 3)	Read specified web resources (Prepare for exam)
Wed	12/9		(Final)	(Prepare for final)

The course schedule, policies, procedures, and assignments in this course are subject to change in the event of extenuating circumstances, by mutual agreement, and/or to ensure better learning.