ECEN 3733 - Digital Circuit Design

Summer 2026 Syllabus, Section 01, CRN 31031,

Credit hours: 3

Instructor

Dr. Guy Gadola

Professional Qualifications:
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Preferred Contact Method: Email or in person

Communication Expectations:
I intend to respond within 24 hours but might not check email on weekends.

Course Description

3733. Digital Circuit Design. Modern digital circuit analysis and design. Latches, flip-flops, registers, counters, memories, programmable logic arrays, and arithmetic logic units. Logic gate-level synthesis and computer simulation using CAD tools. Synchronous and asynchronous finite-state machines. Prereq.: ECEN 1521, ECEN 2633. 3 s.h.

Course Readings

Group	Title	Author	ISBN
Required	Fundamentals of Logic Design, Enhanced Edition. 7th ed.	Roth Jr , Charles; Kinney, Larry; John, Eugene.	9781337620352
Required	Asynchronous Finite State Machine Design: A Lost Art?	Carroll, C.	Academic Paper

ASEE PEER - Asynchronous Finite State Machine Design: A Lost Art?

Carroll, C. (2006, June), *Asynchronous Finite State Machine Design: A Lost Art?* Paper presented at 2006 Annual Conference & Exposition, Chicago, Illinois. 10.18260/1-2--379

The course readings are subject to change in the event of extenuating circumstances, research developments, current events, and/or to ensure better learning.

Schedule of Topics and Assignments

Week of	Reading(s)	Proposed Topic	Due/To Prepare for Class
5/11	Unit 1 Unit 2 Unit 3	Unit 1. Introduction Number Systems and Conversion Unit 2. Boolean Algebra Unit 3. Boolean Algebra (Continued)	
5/18	Unit 4 Unit 5 (Exam 1)	Unit 4. Applications of Boolean Algebra Minterm and Maxterm Expansions Unit 5. Karnaugh Maps	

5/25	Sec. 6.6 Secs. 7.1, 7.2 Unit 8	Sec. 6.6. Quine-McCluskey Method Overview Sec. 7.1. Multi-Level Gate Circuits. Sec. 7.2. NAND and NOR Gates Unit 8. Combinational Circuit Design and Simulation Using Gates
6/1	Unit 9 Unit 10 (Exam 2)	Unit 9. Multiplexers, Decoders, and Programmable Logic Devices Unit 10. Introduction to VHDL
6/8	Sec. 20.2 Unit 11 Asynchronous Finite State Machine Design: A Lost Art? Unit 14	Within Sec. 20.2. VHDL Test Bench and For Loop Unit 11. Latches and Flip-Flops Asynchronous Finite State Machines Unit 14. Derivation of State Graphs and Tables
6/15	Unit 17 Unit 12 (Exam 3)	Unit 17. VHDL for Sequential Logic Unit 12. Registers and Counters
6/22	(Catch-up) (Work on Project) (Final Exam)	

The course schedule, policies, procedures, and assignments in this course are subject to change in the event of extenuating circumstances, by mutual agreement, and/or to ensure better learning.